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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/064,171 | 06/18/2002 | James W. Adkisson | BUR919990299 | 8362 |

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| EXAMINER | |
|---|---|
| MAGEE, THOMAS J | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2811 | |

DATE MAILED: 05/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/064,171 | ADKISSON ET AL. | |
| | Examiner | Art Unit | |
| | Thomas J. Magee | 2811 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *26 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections – 35 U.S.C. 103*

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office Action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1 – 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mizuno et al. (US 5,844,278) in view of Sung (US 5,792,690).

6. Regarding Claim 1, Mizuno et al. disclose an FET semiconductor device (Figure 17) comprising a conduction channel (under gate 56) of dimension equal to 0.1um, corresponding to the width of layer (52) (x-axis in figure) (Col. 14, line 29) ("second width,") formed through a lithographic process. Additionally, Mizuno et al. disclose a "first width," (y-axis) wherein the length is < 0.1 um (from measurements approximated in Figure 17), such that the first width is smaller than the second width corresponding length < 0.1um and defined as "sub-lithographic" with source and drain regions (57,58) and polysilicon gate regions (56) (Col. 4, lines 43 – 45) on opposing sides of the conduction channel. Mizuno et al. do not disclose the presence of silicide sidewalls on polysilicon gates or "offsets" (recesses) from source/drain regions.

Sung discloses the formation of silicide spacers (8) (Figure 3b) (Col. 6, lines 4 – 5) (Col. 1, lines 61 – 63) (Col. 2, lines 7 – 10) (Col. 7, lines 60 – 61) on a polysilicon line trace depos-

ited on a dielectric layer (5) with an ancillary objective (Col. 1, lines 61 – 63) of forming silicide spacers on the sides of polysilicon gate structures to reduce gate resistance. It would then have been obvious to one of ordinary skill in the art at the time of the invention to use the procedure of Sung with an underlying insulating layer (5) and silicide spacer (8) on a polysilicon line in Mizuno et al. to form a silicide spacer at the sidewalls of the polysilicon gate with an underlying insulator (to provide an offset at the source/drain regions) and thereby to reduce gate resistance and avoid shorts. Further, Mizuno et al. disclose (Figures 17 and 18) that the polysilicon gate regions are on opposing sides of the conduction channel and are recessed (Figure 18) from the source/drain regions.

7. Regarding Claim 2, Mizuno et al. do not disclose the presence of silicide spacers at sidewalls in the form of liners. Sung discloses the formation of silicide spacers (8) in the form of liners (Figure 3b) (Col. 6, lines 4 – 5) on a polysilicon line trace deposited on a dielectric layer (5) with an ancillary objective (Col.1, lines 61 – 63) of forming silicide spacers on the sides of polysilicon gate structures to reduce gate resistance. It would then have been obvious to one of ordinary skill in the art at the time of the invention to use the procedure of Sung with an underlying insulating layer (5) and silicide spacer (8) on a polysilicon line in Mizuno et al. to form a silicide spacer in the form of a liner at the sidewalls of the polysilicon gate with an underlying insulator (to provide an offset at the source/drain regions) and thereby to reduce gate resistance and avoid shorts.

8. Regarding Claim 3, Mizuno et al. disclose that the polysilicon gate regions are connected with a polysilicon strip at the top (See Figure 17).

9. Claims 4 – 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mizuno et al. in view of Sung, as applied to Claims 1 – 3, and further in view of Liu et al. (US 6,380,078 B1).

10. Regarding Claims 4 and 5, neither Mizuno et al. or Sung disclose that the connector is a damascene connector. However, Liu et al. disclose a method for forming damascene interconnects (See Figure 2F) wherein trenches are formed in an insulating layer, filled with metal, and the surface planarized (Col. 8, lines 47 – 54). It would have been obvious at the time of the invention to one of ordinary skill in the art to use the method of Liu et al. to form damascene interconnects and to combine Liu et al. with Mizuno et al. and Sung to reduce the delay associated with resistance and capacitance of the interconnect structure.

11. Regarding Claims 6 – 8, neither Mizuno et al. or Sung disclose that the silicide sidewalls are connected or that the connector is a damascene connector formed within a trench in the insulating region. However, Liu et al. disclose a method for forming damascene interconnects (See Figure 2F) wherein trenches are formed in an insulating layer, filled with metal, and the surface planarized (Col. 8, lines 47 – 54). It would have been obvious at the time of the invention to one of ordinary skill in the art to use the method of Liu et al. to form damascene interconnects and to combine Liu et al. with Mizuno et al. and Sung to reduce the delay associated with resistance and capacitance of the interconnect structure.

### *Response to Arguments*

13. Arguments of Applicant have been carefully considered but have been found to be unpersuasive.

Arguments regarding the definition of "sublithographic" remain peripheral. The "dimensions" of "sublithographic" are changing and what was defined as such ten years ago is not the same as today. Further, the definition has changed even since the instant application was filed in 2002. Additionally, "sublithographic" refers to a process step and is not an appropriate device (structural) limitation. Therefore, dimensions must be provided and should be readily available from data acquired by Applicant. Applicant has repeatedly failed to provide definitive dimensions on his invention, and this has tended to delay prosecution of the application.

In regard to the formation of tungsten silicide spacers, Applicant has recited one embodiment stating the use of tungsten. However, the reference recites the use of either tungsten or tungsten silicide (Col. 2, lines 7 – 10, Col. 3, lines 18 – 34, Col. 6, lines 4 – 5).

### *Conclusions*

17. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to **Thomas Magee**, whose telephone number is **(571) 272 1658.** The Examiner can normally be reached on Monday through Friday from 8:30AM to 5:00PM (EST). If attempts to reach the Examiner by telephone are unsuccessful, the examiner's supervisor, **Eddie Lee**, can be reached on **(571) 272-1732.** The fax

number for the organization where this application or proceeding is assigned is **(703)**

**872-9306.**

Thomas Magee
April 26, 2004

EDDIE LEE
SUPERVISORY PATENT EXAMINER
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